REMARKS

The Examiner's Action mailed on August 10, 2005 has been received and its contents carefully considered. Claim 4 has been amended. Claims 1-17 are now pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Claims 4 and 5 are rejected under 35 U.S.C. 112, second paragraph. Claim 4 has been amended to rename "the constriction variable resistor" to "the transistor". Withdrawal of the rejection is requested.

Claims 1-11, 14, and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by *Jain* (US Patent 6,275,088). It is submitted that claim 1 clearly is patentable over *Jain* for at least the following reasons.

Applicant's independent claim 1 recites:

> Claim 1 (Previously presented): An apparatus of ring-back constriction, coupled to a transmission line, for constricting a ring-back effect, the apparatus comprising:
>
> a comparator, coupled to the transmission line, for comparing a line signal of the transmission line with a reference voltage, and accordingly outputting a comparison signal;
>
> a termination controller, coupled to the comparator, for outputting a termination control signal according to the comparison signal;
>
> a termination variable resistor, coupled to a termination voltage and the transmission line, the resistance of the termination variable resistor being adjusted according to the termination control signal for providing a voltage to the transmission line;
>
> a constriction controller, coupled to the comparator, for outputting a constriction signal; and
>
> a transistor, having a gate and a source, the gate receiving the constriction signal, the transistor being coupled to a constriction voltage and the transmission line, the resistance of the transistor being adjusted according to the voltage difference between the gate and the source;

wherein when the level of the line signal changes from a first voltage level to a second voltage level, the level of the constriction signal successively changes from a third voltage level to a fourth voltage level, maintains the fourth voltage level for a period, and returns to the third voltage level."

Jain recites:

"Turning now to FIG. 5, a schematic diagram of one embodiment of the clamping circuit 22 is illustrated. The transmission line 16 is connected to an input buffer 36, which is comprised of two inverters 50, 51" (emphasis added; see *Jain*'s col. 4, lines 7 to 10, and Fig. 5)

The Examiner asserts (page 3, lines 7-9) that *Jain*'s input buffer 36, which is comprised of two inverters 50, 51, anticipates the comparator defined in claim 1, because each gate has an "intrinsic threshold or reference voltage defined by the manufacturing of the [inverter]." However, the Examiner is invited consider that *Jain*'s inverter 50 only can output a voltage level inverse to the voltage level on the transmission line 16, and *Jain*'s inverter 51 only can output a voltage level inverse to the voltage level of the output on the inverter 50; because of this double inversion, *Jain*'s input buffer 36 output voltage is the same as its input voltage.

A "buffer" is believed to be a device for matching impedance or current loads, not a device for changing voltage or detecting any condition, and a buffer is an electrical component quite different from a comparator. A buffer only has one input end, and the output voltage level of a buffer corresponds only to the input voltage level of the buffer. However, a comparator has two input ends for comparing, and the output voltage level of a comparator corresponds to the difference between the voltage levels at the two input ends. If a reference voltage is input to one input end of the comparator, the reference voltage can be selected to accommodate the design, but the buffer does not

have this ability. A buffer has different structure, a different function, and a different operation than a comparator. Therefore, a comparator can not be anticipated by a buffer.

With respect, the "intrinsic threshold or reference voltage" asserted by the Examiner (1) is not disclosed, and (2) would be irrelevant if it were disclosed.

(1) The inverters 50, 51 are only mentioned in the text in the cited passage (col. 4, line 10) and nowhere else, so the only description is "inverter" and Fig. 5 comprises the main disclosure on these inverters. Fig. 5 shows that the inverters are straight-forward inverting amplifiers, and the schematic is simplified so that only the input and output are shown: the powering voltage and the ground are omitted, but those skilled in the art will know that the inverting amplifiers must have power, and must be connected to ground. And they will also understand that the input signal is referenced to ground, which is *always* the reference when no other reference is specified.

Therefore, the disclosure of *Jain* is that the "intrinsic ... reference voltage," if there is one (not admitted), must be ground potential. Ground can be a reference voltage (as can any other voltage), but when the instant claim *mentions* a reference voltage, the person skilled in the art will *not* take that as meaning ground (just as a geographer will understand "an elevation of 300 feet" to mean 300 feet above mean sea level, but will not take "an elevation 300 feet above a reference elevation" to mean the same thing, because the mere mention of the reference elevation means that it is not sea level, but some other special reference elevation.)

The *output* of a comparator is referenced to ground, but the *input* is referenced to some other voltage; otherwise, the "comparator" would degenerate into a "buffer."

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(2) The Examiner's asserted "intrinsic threshold ... voltage defined by the manufacturing of the [inverter]" is, with respect, immaterial. The components of the inverting amplifiers 50 and 51 will of course have intrinsic thresholds, but these will not affect the operation of the buffer 36; if they do, the buffer is faulty.

For example, the transistors of the buffer 36 might have a minimum turn-on voltage, but the amplifier design should take this into account, and obviate it, in order to avoid signal distortion. If the inverting amplifiers 50 and 51 are operating normally and properly, no intrinsic threshold should affect their performance.

Therefore, the "comparator, coupled to the transmission line, for comparing a line signal on the transmission line with a reference voltage, and accordingly outputting a comparison signal" as recited in the claim 1 is not disclosed by *Jain*, and therefore claim 1 is not anticipated by *Jain*.

Claims 2-16 depend from claim 1, and therefore are patentable for at least the reasons advanced above as to the patentability of claim 1. Claim 17 is also patentable based on the same arguments for claim 1 given above. Allowance is requested.

Respectfully submitted,

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Date

Nick Bromer (Reg. No. 33,478)
(717) 426-1664
RABIN & BERDO, P.C.
CUSTOMER NO. 23995
Telephone: (202) 371-8976
Telefax: (202) 408-0924